Microprocessor Data Book

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FERRANTI F100L

The Ferranti F100L is a 16-bit bipolar microprocessor which uses the Ferranti CDI process for fabrication. It is the only microprocessor to have been developed in Europe and is one of the few processors with full military specifications, although some other types do meet the military temperature range.

The general design of the F100L follows that of the Ferranti minicomputers and tends to be somewhat simpler than that of the newer 16-bit *n*MOS microprocessors such as the MC68000 and Z8000.

In terms of computing power the F100L is very flexible, but possibly not as powerful as the 68000 or Z8000 types. Compared with these processors, which can access megabytes of memory, the F100L allows only 32k words, which is however perfectly adequate for virtually all small to medium size applications. The F100L also has a rather less comprehensive instruction set compared with other processors, and requires an external chip for hardware multiply and divide functions. Speed of operation is comparable with that of other types of 16-bit microprocessor.

Prime manufacturer

Ferranti Ltd.

Devices available

F100L Basic 16-bit microprocessor chip

Alternative source devices

None at present.

Architecture

As will be seen from fig. 4.2 the internal architecture of the F100L is extrememly simple with virtually no working registers.

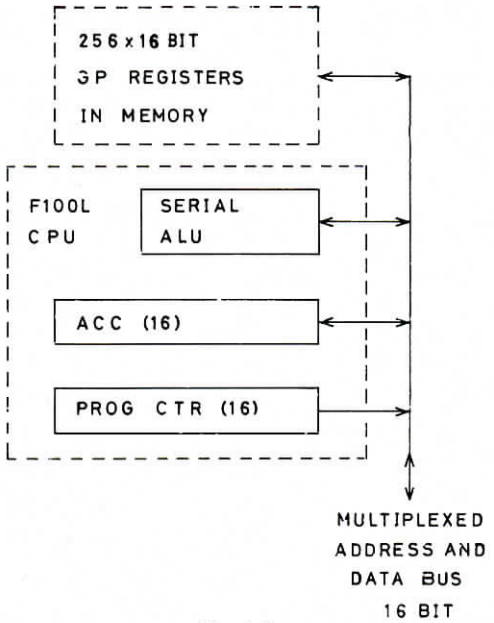

Fig. 4.2

A 16-bit accumulator and arithmetic and logic unit (ALU) deals with the main processing functions. An interesting feature is that the ALU operates in bit serial mode rather than parallel as in other microprocessors. There is also a status register for condition flags and processor status.

The program counter has 15 bits, to provide addressing of up to 32k words of external memory.

No index registers or stack pointers are provided on the CPU itself, since these are implemented within the first 256 words of the external memory. Thus the processor can have up to 256 directly accessible working registers in external memory. These may also be used as data pointers for indirect and indexed addressing.

A 16-bit multiplexed data and address bus is used to communicate with memory and input–output devices.

Package

40-pin dual in line type ceramic

Power requirements

V_{cc}	+5 V ± 5%
V_{ss}	0 V
Supply current	270 mA

Temperature range

Commercial type	0°C to +70°C
Industrial type	−40°C to +85°C
Military type	−55°C to +125°C

Input–output

The F100L uses a common address space for memory and input–output devices. When a data transfer is to occur the F100L outputs the address of the source or destination device and indicates the direction of data flow. The device must then produce a handshake signal, following which data transfer occurs over the common multiplexed 16-bit bus.

Facilities are provided for direct memory access when the F100L is not using the bus. A DMA request is input to the CPU and when acknowledged by the F100L the bus is released for use by external devices.

External devices are interfaced to the bus via a set of three interface chips. They provide control, data and memory interfaces to the processor bus system.

Interrupt facilities

A single maskable interrupt line is provided on the F100L. On receipt of an interrupt request the CPU saves the contents of the program counter and status register on a stack located within the memory system. The stack pointer is location 0 of the main memory. The CPU then issues an interrupt acknowledge output and expects to receive from the interrupting device a 16-bit vector address, from which the CPU will pick up the start address of the interrupt service routine. These vector addresses are located either from location 2048 or location 16384 in memory, forming a table of up to 64 vectors. Vector 0 is shared with the reset/start vector and some care must be exercised if this is used for interrupt routines.

There is no interrupt priority system and therefore any priority scheme must be handled by external hardware.

Instruction set

There are 153 different instructions in the F100L set, which may be grouped as 28 types of operation.

Arithmetic and logic
For 16-bit arithmetic operations both addition and subtraction are provided and may be executed either with or without carry. Double length (32 bit) arithmetic operations may also be used on the F100L. An interesting feature is that in subtraction the accumulator contents are subtracted from memory contents and the result may be placed either in memory or accumulator as required.

There are no direct instructions for dealing with BCD numbers or for multiplication and division, so these functions must be programmed by software.

Logical operations provided are AND and EXCLUSIVE OR as well as a selection of shift and rotate operations, some of which operate on double length words. There is no logical OR function provided. Other operations include compare, increment and decrement.

Data transfers
All data transfers are effectively between the accumulator and either memory or input–output devices, since the registers are located in the lower 256 words of memory.

The stack is not used for data in the F100L. Its use is reserved for subroutine and interrupt operations, where the program counter and status register contents are saved.

Branch and jump
There are 23 branch and jump operations, of which 12 are conditional. Four subroutine call instructions are included with different addressing modes, and all are unconditional. During subroutine calls the program counter and status register are pushed to the stack.

Addressing modes
The F100L supports four basic addressing modes, which are direct, immediate, immediate indirect and pointer indirect. The last mode may be used for indexing with autoincrement or with autodecrement.

Timing

The F100L requires an external clock generator and normally runs with a 20 MHz clock, to give instruction execution times of the order 3 – 4 μs.

Support chips

Several support chips have been specially designed for use with the F100L type CPU:

F111-L	Control interface chip
F112L	Data interface chip
F113L	Memory interface chip, high speed type
F114L	Memory interface chip, low speed type and low power
F101L	Hardware multiplier and divider
F115L	Timer and interrupt controller
F116L	Timer chip
F117	Interrupt controller
ZN1001	Clock generator for F100L

Development aids

Ferranti produce a comprehensive development system for the F100L, which uses a floppy disk based operating system and can provide full hardware and software development and debugging facilities. This is the FDS10 development system, which can also support the real time language CORAL66. F100 resident software includes a text editor, assembler and link editor.